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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,875	09/29/2003	Mahesh J. Deshmane	42P17507	6817

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EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 10/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,875	DESHMANE ET AL.	
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4-11, 13-22, 24 and 26-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received September 26, 2006 for application number 10/675,875 originally filed September 29, 2003. The Office hereby acknowledges receipt of the following and placed of record in file: amended claims 1-28 are presented for examination wherein claims 2, 3, 12, 23 and 25 are canceled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10, 18-22, 24 and 26-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Jenkins, IV (U.S. Patent No. 6,184,708 B1) (hereinafter referred to as Jenkins).

As to claim 1, Jenkins discloses a computer system comprising: a bus (106); and, a chipset (101), coupled to the bus (as shown in Fig. 3), having: an input/output (I/O) buffer (211), coupled to the bus (as shown in Fig. 3), to transmit an output signal (test signal) from the chipset via the bus (column 4, lines 65 thru column 5, lines 11); a slew rate detection mechanism (216 in combination with 104), coupled to the bus (as shown in Fig. 3), to detect a slew rate of the output signal transmitted from the I/O buffer and to generate a signal indicating a status of the slew rate (Jenkins discloses the output buffer 211 sending out a test signal to device 102 via bus 106 and sent back an received at input buffer 212 to detect the test signal at asynchronous latch 216 to be

used by configuration processor 104 to create slew correction data to be used by the slew rate control 213; column 6, lines 41-52 and column 7, line 16-23 and column 7, lines 38-65); and, control logic (213), coupled to the slew rate detection mechanism (as shown in Fig. 3), to receive the signal and to adjust the slew rate based upon the state of the signal (column 5, lines 25-26).

As to claim 4, Jenkins further discloses the computer system of claim 1 wherein the control logic reduces the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too fast (column 7, lines 50-65).

As to claim 5, Jenkins further discloses the computer system of claim 1 wherein the control logic increases the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too slow (column 2, lines 42-56).

As to claim 6, Jenkins further discloses the computer system of claim 1 wherein the slew rate detection mechanism includes a capacitor, coupled to the bus, to integrate the received signal current (By the relationship of $Z_c = \frac{V_R}{I_R} = \frac{1}{j\omega C}$ as is known in the art; column 5, lines 12-25).

As to claims 7-9, they are directed to the computer system of steps set forth in claim 6. Therefore, they are rejected for the same basis as set forth hereinabove.

As to claim 10, Jenkins further discloses the computer system of claim 1 wherein the bus is a high-speed bus (column 1, lines 38-43).

As to claim 18, Jenkins discloses a method comprising: transmitting a signal (test signal) from an input/output (I/O) buffer (211) within a chipset (101) over a bus (106) (Fig. 3 and column 4, lines 65 thru column 5, lines 11); receiving the signal at a slew rate detection mechanism (216 in combination with 104) within the chipset via the bus (Jenkins discloses the output buffer 211 sending out a test signal to device 102 via bus 106 and sent back an received at

input buffer 212 to detect the test signal at asynchronous latch 216 to be used by configuration processor 104 to create slew correction data to be used by the slew rate control 213; column 6, lines 41-52 and column 7, line 16-23 and column 7, lines 38-65); generating a signal indicating the status of the slew rate (column 7, lines 50-65); and, adjusting the slew rate at control logic (213) within the chipset based upon the signal (column 5, lines 26-39 and column 6, line 42 thru column 7, line 4).

As to claim 19, Jenkins further teaches the method of claim 18 further comprising generating a reference current at the chipset (By the relationship of $Z_c = \frac{V_R}{I_R} = \frac{1}{j\omega C}$ as is known in the art; column 5, lines 12-25).

As to claim 20, it is directed to the method of steps set forth in claim 19. Therefore, it is rejected for the same basis as set forth hereinabove.

As to claim 21, Jenkins further teaches the method of claim 18 wherein adjusting the slew rate comprises modifying the amplification of a second signal at the I/O buffer (column 5, lines 26-49).

As to claim 22, Jenkins discloses an apparatus comprising: an input/output (I/O) buffer (211) to transmit an output signal (column 4, lines 65 thru column 5, lines 11); and, a slew rate detection mechanism (216 in combination with 104) coupled (as shown in Fig. 3) to receive the output signal from the I/O buffer via a bus, to detect the slew rate of a the output signal transmitted from the I/O buffer a memory controller over a bus and to generate a signal to indicate the status of the slew rate (Jenkins discloses the output buffer 211 sending out a test signal to device 102 via bus 106 and sent back an received at input buffer 212 to detect the test signal at asynchronous latch 216 to be used by configuration processor 104 to create slew

correction data to be used by the slew rate control 213; column 5, lines 25-26 and column 6, lines 41-52 and column 7, line 16-23 and column 7, lines 38-65).

As to claim 24, Jenkins further teaches the apparatus of claim 22 further comprising control logic, coupled to the I/O buffer and the slew rate detection mechanism, to receive the signal and modify the slew rate based upon the signal.

As to claim 26, Jenkins further teaches the apparatus of claim 22 wherein the slew rate detection mechanism includes a capacitor, coupled to the bus, to integrate the received signal current (By the relationship of $Z_c = \frac{V_R}{I_R} = \frac{1}{j\omega C}$ as is known in the art; column 5, lines 12-25).

As to claims 27 and 28, they are directed to the apparatus of steps set forth in claim 26. Therefore, they are rejected for the same basis as set forth hereinabove.

Claims 11, and 13-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. (U.S. Patent No. 6,477,592 B1) (hereinafter referred to as Chen).

As to claim 11, Chen discloses a computer system comprising: a main memory device (20); a memory bus (data, address, control bus) coupled to the main memory device (Figs. 3, 4 and 5); and, a memory controller (22), coupled to the bus, having: an input/output (I/O) buffer (44), coupled to the bus (as shown in Fig. 5), to transmit an output signal from the memory controller via the bus (column 12, line 56 thru column 13, line 3); a slew rate detection mechanism (56), coupled to the bus (as shown in Fig. 5), to detect a slew rate of the output signal transmitted from the I/O buffer and to generate a signal indicating a status of the slew rate (column 11, line 65 thru column 12, line 13); and, control logic (56), coupled to the slew rate detection mechanism, to receive the signal and to adjust the slew rate based upon the state of the signal (Chen discloses the slew rate controller 56 having the ability to both determine the slew

rate in addition to sending the slew correction signals to the driver 58 wherein both slew control 56 and driver are within buffer 44; column 11, line 65 thru column 12, line 13) (Chen further discloses the details of all the components within the memory chip 20, access hub 18 and memory controller 22 all having the same operational functionality; column 13, lines 32-39).

As to claim 13, Chen further teaches the computer system of claim 11 wherein the control logic reduces the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too fast (Chen discloses increasing or decreasing slew transition dependent on measure slew rate; column 11, line 65 thru column 12, line 21).

As to claim 14, Chen further teaches the computer system of claim 11 wherein the control logic increases the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too slow (Chen discloses increasing or decreasing slew transition dependent on measure slew rate; column 11, line 65 thru column 12, line 21).

As to claim 15, Chen further teaches the computer system of claim 11 wherein the slew rate detection mechanism includes a capacitor, coupled to the bus, to integrate the received signal current (column 17, lines 32-54).

As to claims 16 and 17, they are directed to the computer system of steps set forth in claim 15. Therefore, they are rejected for the same basis as set forth hereinabove.

Response to Arguments

Applicant's arguments with respect to claims 1, 4-11, 13-22, 24 and 26-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The Examiner can normally be reached on 8AM - 4PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (IN USA OR CANADA) or (571) 272-1000.

James F. Sugent
Patent Examiner, Art Unit 2116
October 4, 2003

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